

CLAIMS

What is claimed is:

1           1.    A method for forming multiple resistors on a  
2    substrate, comprising:  
3           first providing a first resistor;  
4           first depositing, patterning, and selectively etching a  
5    first dielectric layer over the first resistor;  
6           second providing second resistor material over the first  
7    dielectric layer;  
8           third providing landing pad material over the second  
9    resistor material; and  
10          selectively etching said landing pad material and said  
11    second resistor material, where said selectively etching  
12    forms contacts for the first resistor in a first region, and  
13    forms a second resistor and associated contacts in a second  
14    region.

1           2.    The method of claim 1, wherein said first providing  
2    includes providing chromium silicon (CrSi) material.

1           3.    The method of claim 1, wherein said first providing  
2    includes providing nickel chromium (NiCr) material.

1           4.    The method of claim 1, wherein said first providing  
2 includes providing a silicon substrate.

1           5.    The method of claim 1, wherein said second  
2 providing includes providing nickel chromium (NiCr) material.

1           6.    The method of claim 1, wherein said third providing  
2 said landing pad material includes providing titanium-nitride  
3 (TiN).

1           7.    The method of claim 1, wherein said third providing  
2 said landing pad material includes providing titanium-  
3 tungsten (TiW).

1           8.    The method of claim 1, wherein said first providing  
2 a first resistor includes providing a substrate.

1           9.    The method of claim 8, wherein said first providing  
2 a first resistor includes depositing a second dielectric  
3 layer on top of the substrate.

1        10. The method of claim 9, wherein said first providing  
2        a first resistor includes depositing, patterning, and  
3        selectively etching a first resistor material on top of the  
4        second dielectric layer.

1        11. The method of claim 1, further comprising:  
2        second depositing a second dielectric layer on said  
3        contacts for the first resistor, exposed portions of said  
4        second resistor, and exposed portions of said first  
5        dielectric layer.

1        12. The method of claim 11, further comprising:  
2        appropriately repeating said first providing, said first  
3        depositing, said second providing, said third providing, said  
4        selectively etching, and said second depositing.

1        13. A method for forming a plurality of thin film  
2 resistors, comprising:  
3        forming a first thin film resistor;  
4        depositing and selectively etching a dielectric layer to  
5 provide contact openings for the first thin film resistor;  
6        patterning and selectively etching landing pad material  
7 on a layer of second thin film resistor material in the  
8 contact openings to provide contacts to the first thin film  
9 resistor;

10       first selectively etching the landing pad material on  
11 the layer of the second thin film resistor material at an  
12 area away from the contact openings to form a second thin  
13 film resistor; and  
14       second selectively etching the landing pad material  
15 above the second thin film resistor to expose the second thin  
16 film resistor, and to provide contacts for the second thin  
17 film resistor.

1        14. The method of claim 13, further comprising:  
2        appropriately repeating said forming, said depositing,  
3 said patterning, said first selectively etching, and said  
4 second selectively etching, to form additional thin film  
5 resistors.

1        15. A method for forming a plurality of thin film  
2 resistors, comprising:  
3        first providing a substrate;  
4        first depositing a first dielectric layer on the  
5 substrate;  
6        second depositing a first thin film resistor material on  
7 the first dielectric layer;  
8        first patterning and selectively etching the thin film  
9 resistor material to form a first thin film resistor;  
10       third depositing a second dielectric layer over the  
11 first thin film resistor and over the exposed portion of the  
12 first dielectric layer;  
13       etching the second dielectric layer over portions of the  
14 first thin film resistor to provide contact openings for the  
15 first thin film resistor;  
16       fourth depositing second thin film resistor material  
17 over portions of the first thin film resistor underlying the  
18 contact openings and over the second dielectric layer;  
19       fifth depositing landing pad material over the second  
20 thin film resistor material;  
21       second patterning and selectively etching the landing  
22 pad material and the second thin film resistor material over  
23 the contact openings to provide etch-stop contacts for the  
24 first thin film resistor;

25       third patterning and selectively etching the landing pad  
26 material and the second thin film resistor material at an  
27 area away from the first thin film resistor to form a second  
28 thin film resistor;

29       selectively etching the landing pad material on the  
30 second thin film resistor to expose the second thin film  
31 resistor, and to provide contacts to the second thin film  
32 resistor with remaining portions of the landing pad material;

33       sixth depositing a third dielectric layer over the  
34 etched landing pad material, exposed portion of the second  
35 thin film resistor, and exposed portion of the second  
36 dielectric layer; and

37       second providing shallow contacts to the first and  
38 second thin film resistor.

1       16. The method of claim 15, wherein said providing a  
2 substrate includes providing a silicon substrate.

1        17. An integrated circuit structure having thin film  
2 resistors, comprising:

3        a first dielectric layer;

4        a first thin film resistor disposed on said first  
5 dielectric layer over a first region;

6        a second dielectric layer disposed on said first  
7 dielectric layer and said first thin film resistor;

8        a plurality of contacts for the first thin film resistor  
9 having at least first and second layers, the first layer  
10 including second thin film resistor material, and the second  
11 layer including landing pad material, said plurality of  
12 contacts disposed on top edge portions of the first thin film  
13 resistor; and

14       a second thin film resistor having at least first and  
15 second layers, the first layer including said second thin  
16 film resistor material, and the second layer including said  
17 landing pad material, said second thin film resistor disposed  
18 on the second dielectric layer over a second region.

1       18. The method of claim 17, further comprising:

2       a third dielectric layer deposited on said plurality of  
3 contacts for the first thin film resistor, exposed portions  
4 of said second thin film resistor, and exposed portions of  
5 said second dielectric layer.

1        19. The method of claim 18, further comprising:

2        a plurality of metal contacts in the third dielectric  
3 layer, said metal contacts coupled to the first and second  
4 thin film resistors.

1        20. An integrated circuit including a plurality of thin  
2 film resistors, comprising:

3        a plurality of integrated structures, each structure  
4 successively disposed on top of a previous structure, each  
5 structure including:

6                a first dielectric layer;

7                a first thin film resistor disposed on said first  
8 dielectric layer over a first region;

9                a second dielectric layer disposed on said first  
10 dielectric layer and said first thin film resistor;

11               a plurality of contacts for the first thin film  
12 resistor having at least first and second layers, the  
13 first layer including second thin film resistor  
14 material, and the second layer including landing pad  
15 material, said plurality of contacts disposed on top  
16 edge portions of the first thin film resistor;

17               a second thin film resistor having at least first  
18 and second layers, the first layer including said second  
19 thin film resistor material, and the second layer  
20 including said landing pad material, said second thin



21 film resistor disposed on the second dielectric layer  
22 over a second region; and  
23 a third dielectric layer deposited on said  
24 plurality of contacts for the first thin film resistor,  
25 exposed portions of said second thin film resistor, and  
26 exposed portions of said second dielectric layer.